Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2018

IT3CO04 Computer System Organization

Programme: B.Tech. Branch/Specialisation: IT

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. ..... is used to store data in registers. **1**

(a) D Flip flop (b) JK Flip Flop

(c) RS Flip flop (d) None of these

ii. Which of the register/s of the processor is/are connected to Memory Bus? **1**

(a) PC (b) MAR (c) IR (d) Both (a) and (b)

iii. The instruction, Add #45, R1 does..... **1**

(a) Adds the value of 45 to the address of R1 and stores 45 in that address

(b) Adds 45 to the value of R1 and stores it in R1

(c) Finds the memory location 45 and adds that content to that of R1

(d) None of these

iv. The CISC stands for..... **1**

(a) Computer Instruction Set Compliment

(b) Complete Instruction Set Compliment

(c) Computer Indexed Set Components

(d) Complex Instruction set computer

v. The Flag 'V' is set to 1 indicates that..... **1**

(a) The operation is valid

(b) The operation is validated

(c) The operation as resulted in an overflow

(d) None of these

P.T.O.

vi. The access time of memory is …… the time required for performing any single CPU operation. **1**
(a) Longer than (b) Shorter than
(c) Negligible than (d) Same as

vii. The system is notified of a read or write operation by **1**
(a) Appending an extra bit of the address
(b) Enabling the read or write bits of the devices
(c) Raising an appropriate interrupt signal
(d) Sending an special signal along the BUS

viii. The DMA transfers are performed by a control circuit called as **1**
(a) Device Interface (b) DMA Controller
(c) Data Controller (d) Overlooker

ix. Each stage in pipelining should be completed within .....cycle. **1**
(a) 1 (b) 2 (c) 3 (d) 4

x. In Flynn's taxonomy, Super Computer is based on..... Structure. **1**
(a) SISD (b) SIMD (c) MISD (d) MIMD

Q.2 i. What is a register? Explain the function of MAR, PC, IR & MBR. **2**
ii. What is Von Neumann model? Write down the functional block of the Von Neumann computer model. **3**
iii. What is Instruction cycle? Draw the fetch, decode and execute phase of instruction cycle. **5**
OR iv. What is Instruction format? Explain the types of instruction formats with an example. **5**

Q.3 i. Differentiate between RISC and CISC computer. **3**
ii. What is addressing modes? Explain the types of addressing modes. **7**
OR iii. What is stack based organization? Write a program to evaluate following arithmetic expression in one-address, zero-address instruction format :- X=(A+B)*(C+D) **7**

Q.4 i. What is memory hierarchy? Discuss with the speed and cost parameter? **3**

ii. Show the Step by step multiplication process using booth's algorithm for the following number:- multiplicand is (-23) and multiplier is (+19). **7**
OR iii. A digital computer has a memory unit of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. **7**
(a) How many bits are there in the tag, index, block and word fields of the address format?
(b) How many bits are there in each word of cache and how are they divided into Functions? Include a valid bit.
(c) How many blocks can the cache accommodate.

Q.5 i. What is serial and parallel data transmission? Explain the handshaking method for asynchronous data transfer? **4**
ii. What is Input-Output Interface? Draw and explain the Asynchronous communication interface? **6**
OR iii. What do you mean by initialization of DMA controller? How does DMA controller work? Explain with suitable block diagram? **6**

Q.6 Attempt any two:
i. What is pipeline processing? Explain the arithmetic pipelining with the help of an example. Also draw the space time diagram for a four segment pipeline showing the time it takes to process eight tasks. **5**
ii. What is an Array processor? Describe the types of Array processor? **5**
iii. A Non- pipelined system takes 100 ns to process a task. The same task can be processed in a six segment pipeline with a clock cycle of 20 ns. Determine the speedup ratio of the pipeline for 200 tasks. What is the maximum speed up that can be achieved? **5**

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Marking Scheme
IT3CO04 Computer System Organization

Q.1 i. ..... is used to store data in registers. **1**
(a) D Flip flop

ii. Which of the register/s of the processor is/are connected to Memory Bus? **1**
(b) MAR

iii. The instruction, Add #45, R1 does..... **1**
(b) Adds 45 to the value of R1 and stores it in R1

iv. The CISC stands for..... **1**
(d) Complex Instruction set computer

v. The Flag 'V' is set to 1 indicates that..... **1**
(c) The operation as resulted in an overflow

vi. The access time of memory is …… the time required for performing any single CPU operation. **1**
(a) Longer than

vii. The system is notified of a read or write operation by **1**
(d) Sending an special signal along the BUS

viii. The DMA transfers are performed by a control circuit called as **1**
(b) DMA Controller

ix. Each stage in pipelining should be completed within .....cycle. **1**
(a) 1

x. In Flynn's taxonomy, Super Computer is based on..... Structure. **1**
(d) MIMD

Q.2 i. Definition of register 1 mark **2**
Function of each register that given in question
0.25 mark each (0.25*4 = 1 mark)

ii. Von Neumann model 1 mark **3**
subsystem of the von neumann computer model 2 marks

iii. Instruction cycle 2 marks **5**
Flowchart of the fetch, decode and execute phase of instruction cycle(Basic Cycle) 3 marks

OR iv. Definition of Instruction format 1 mark **5**
Types of instruction formats with an example. 4 marks
1 mark each type (1 mark *4)

Q.3 i. Differentiate between RISC and CISC computer. **3**
0.5 Marks for each difference (0.5 mark *6)

ii. Defining the addressing modes 1 mark **7**
Types of addressing modes (0.5 mark each) 6 marks

OR iii. Stack based organization 3 marks **7**
Evaluate arithmetic expression in one-address instruction format 2 marks
Evaluate arithmetic expression in zero-address instruction format 2 marks

Q.4 i. Memory hierarchy 2 marks **3**
Discuss with the speed and cost parameter 1 mark

ii. Booth's algorithm. 3 marks **7**
Showing algorithm 4 marks

OR iii. Describing direct mapping in cache memory. 2 marks **7**
For right answer of (a) 2 marks
For right answer of (b) 2 marks
For right answer of (c) 1 mark

(a) How many bits are there in the tag, index, block and word fields of the address format?

Answer: 64K*16 = 16-bit data and 16 bit- address

6 bit	8 bit	2 bit
Tag	Block	Word
	Index	= 10-bit cache address

(b) How many bits are there in each word of cache and how are they divided into Functions? Include a valid bit.

Answer :

1 bit	6 bit	16 bit	= 23 bits in each word of the cache
Valid	Tag	Data	

(c) How many blocks can the cache accommodate.

Answer:

2^8 = 256 Blocks of 4 words each.A digital computer has a memory unit of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words

Q.5	i.	Serial and parallel data transmission	2 marks	**4**
		Handshaking method for asynchronous data transfer	2 marks	
	ii.	Input-Output Interface with reason	2 marks	**6**
		Diagram of the Asynchronous communication interface	2 marks	
		Explanation of the Asynchronous communication interface	2 marks	
OR	iii.	Suitable block diagram.	3 marks	**6**
		Initialization of DMA controller and How does DMA controller work.	3 marks	
Q.6		Attempt any two:		
	i.	Defining pipeline processing.	1 mark	**5**
		Describing the arithmetic pipelining with example	2 marks	
		Diagram for a four segment pipeline showing the time it takes to process eight tasks	2 marks	
	ii.	Array processor	1 mark	**5**
		2 marks for each Types of Array processor	4 marks	
	iii.	Determine the speedup ratio of the pipeline for 200 tasks	3 marks	**5**
		Calculating the maximum speed up that can be achieved	2 marks	

Solution :

$$S = \frac{nt_n}{(k+n-1)t_p}$$

Where k=6, tn=100 ns, n = 200 , t_p=20 ns

$$S = \frac{200*100}{(6+200-1)*20} = 4.8780 \text{ Ans}$$

$$S_{max.} = \frac{t_n}{t_p} = \frac{100}{20} = 5 \text{ Ans.}$$

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