Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2017

EE3CO09 / EX3CO09 Electronic Devices and Digital Circuits

Programme: B.Tech. Branch/Specialisation: EE/EX

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. $I_C = \beta I_B +$ …….. **1**

(a) I_{CBO} (b) I_C (c) I_{CEO} (d) αI_E

ii. If the value of α is 0.9, then value of β is …….. **1**

(a) 9 (b) 0.9 (c) 900 (d) 90

iii. In an unregulated power supply, if input a.c. voltage increases, the output voltage ……. **1**

(a) Increases (b) Decreases

(c) Remains the same (d) None of these

iv. A Zener diode is used as a voltage regulating device **1**

(a) Shunt (b) Series (c) Series-shunt (d) None of these

v. One condition for oscillation is ……. **1**

(a) A phase shift around the feedback loop of 180^o

(b) A gain around the feedback loop of one-third

(c) A phase shift around the feedback loop of 0^o

(d) A gain around the feedback loop of less than 1

vi. In Colpitt's oscillator, feedback is obtained……. **1**

(a) By magnetic induction

(b) By a tickler coil

(c) From the centre of split capacitors

(d) None of these

vii. How is a J-K flip-flop made to toggle? **1**

(a) J = 0, K = 0 (b) J = 1, K = 0

(c) J = 0, K = 1 (d) J = 1, K = 1

P.T.O.

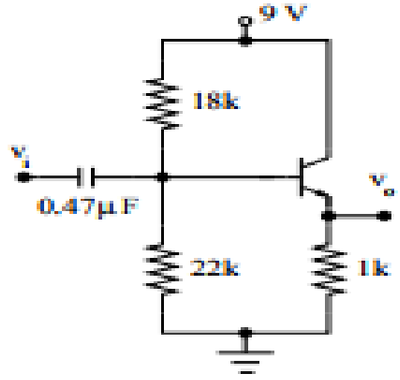
viii. How many flip-flops are required to make a MOD-32 binary counter? **1**
(a) 3 (b) 4 (c) 32 (d) 5

ix. A 4-bit R/2R digital-to-analog (DAC) converter has a reference of 5 volts. What is the analog output for the input code 0101? **1**
(a) 0.3125 V (b) 3.125 V (c) 0.78125 V (d) –3.125 V

x. What is the major advantage of the R/2R ladder digital-to-analog (DAC), as compared to a binary-weighted digital-to-analog DAC converter? **1**
(a) It only uses two different resistor values.
(b) It has fewer parts for the same number of inputs.
(c) Its operation is much easier to analyze.
(d) The virtual ground is eliminated and the circuit is therefore easier to understand and troubleshoot

Q.2 i. Draw and explain the Ebers Moll model for PNP transistor. **4**

ii. Find the I_B and V_{CE} for given circuit. (β=200, V_{BE}=0.7v). **6**



OR iii. Draw the common emitter amplifier circuit h model and calculate the input impedance, voltage gain in terms of h parameters. **6**

Q.3 i. Write down the name types of IC regulators. **2**

ii. Draw the op-amp based current limiting circuit and explain its working. **3**

iii. Draw the SMPS regulator circuit diagram and explain their working with various functional block diagrams. **5**

OR iv. Draw the transistor based voltage series and voltage shunt regulators circuit diagram and explain its working. **5**

Q.4 i. What is Barkhausen Criteria for oscillators? **2**

ii. Draw the circuit diagram of phase shift oscillator and explain its Woking principal. **3**

iii. Draw the circuit diagram of active high pass filter and explain it working principal, also derive the gain expression for it. **5**

OR iv. Draw the block diagram of 555 timer and explain its working principal. **5**

Q.5 i. What is race around condition explain and how it remove? **3**

ii. Draw the 4 bit ring counter using D flip flop and explain its working. **7**

OR iv Design mod 10 decade counter using D flip flop. **7**

Q.6 i. Write down any 3 difference between analog and digital systems **2**

ii. Draw the circuit diagram of DAC (digital to analog converter) using R-2R ladder network with 4 bit input and explain its working. **3**

iii Draw the block diagram of dual slop A/D converter and explain its working. **5**

OR iv Explain the working principal of successive approximation A/D converter with block diagram. **5**

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Marking Scheme

Q.1	i.	$I_C = \beta I_B$ + ……..	**1**
		(c) I_{CEO}	
	ii.	If the value of α is 0.9, then value of β is ……..	**1**
		(a) 9	
	iii.	In an unregulated power supply, if input a.c. voltage increases, the output voltage …….	**1**
		(a) Increases	
	iv.	A Zener diode is used as a voltage regulating device	**1**
		(a) Shunt	
	v.	One condition for oscillation is …….	**1**
		(a) A phase shift around the feedback loop of 180^o	
	vi.	In Colpitt's oscillator, feedback is obtained…….	**1**
		(c) From the centre of split capacitors	
	vii.	How is a J-K flip-flop made to toggle?	**1**
		(d) J = 1, K = 1	
	viii.	How many flip-flops are required to make a MOD-32 binary counter?	**1**
		(d) 5	
	ix.	A 4-bit R/2R digital-to-analog (DAC) converter has a reference of 5 volts. What is the analog output for the input code 0101?	**1**
		(b) 3.125 V (d) –3.125 V	
	x.	What is the major advantage of the R/2R ladder digital-to-analog (DAC), as compared to a binary-weighted digital-to-analog DAC converter?	**1**
		(a) It only uses two different resistor values.	
Q.2	i.	Diagram Ebers Moll model for PNP transistor – 2 marks	**4**
		Explanation Ebers Moll model for PNP transistor – 2 marks	
	ii.	Calculation of I_B = 20 GA – 3 marks	**6**
		Calculation of V_{CE} = 5 v - 3 marks	
OR	iii.	Common emitter amplifier circuit h model – 2 marks	**6**
		Calculation input impedance, voltage gain - 4 marks	
Q.3	i.	Types of IC regulators – 0.5 mark each (0.5 mark * 4 = 2 marks)	**2**
	ii.	Op-amp based current limiting circuit – 1 mark	**3**
		It's working. – 2 marks	
	iii.	SMPS regulator circuit diagram – 2 marks	**5**
		Their working with various functional block diagram – 3 marks	
OR	iv.	Transistor based voltage series and voltage shunt regulators circuit diagram - 2 marks	**5**
		Its working – 3 marks	
Q.4	i.	Barkhausen Criteria for oscillators each criteria have 1 mark	**2**
		(1 mark * 2 = 2 marks)	
	ii.	Circuit diagram of phase shift oscillator – 1 mark	**3**
		Its Woking principal – 2 marks	
	iii.	Circuit diagram of active high pass filter – 1 mark	**5**
		Working principal - 2 marks	
		Gain expression for it – 2 marks	
OR	iv.	Block diagram of 555 timer - 2 marks	**5**
		Its working principal – 3 marks	
Q.5	i.	Race around condition – 2 marks	**3**
		How to remove Race around condition – 1 mark	
	ii.	4 bit ring counter circuit – 3 marks	**7**
		Its working – 4 marks	
OR	iv	Decade counter using D flip flop – 3 marks	**7**
		Calculation for counter and explanation – 4 marks	
Q.6	i.	Any 3 difference between analog and digital systems	**2**
	ii.	DAC (digital to analog converter) circuit ladder – 1 mark	**3**
		DAC circuit ladder working – 2 marks	
	iii	Block diagram of dual slop A/D converter – 2 marks	**5**
		Dual slop A/D converter working – 3 marks	
OR	iv	Successive approximation A/D converter with block diagram – 2 marks	**5**
		Working principal of Successive approximation A/D converter – 3 marks	

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