Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Even) Examination May-2018

EC3CO10/ EE3CO08/EI3CO10/ EX3CO08

Microprocessors & Microcontrollers

Programme: B.Tech. Branch/Specialisation: EC/EE/EI/EX

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. In 8085 microprocessor DCR B instruction affects following flags **1**

(a) Sign and Zero flag only (b) Carry and parity flag only

(c) All conditional flags (d) None of conditional flags

ii. In 8085 system, with I/O mapped I/O scheme Full address range for I/O devices and memory is **1**

(a) 256 I/O and 256 memory

(b) 256 I/O and 64K memory

(c) 64K memory and 256 I/O

(d) 256 Input,256 output and 64K memory

iii. In 8086, if content of IP register is 2057H, what will be the content of DS register to locate the physical address 43657H? **1**

(a) 41600 H (b) 4160 H (c) 456AE H (d) 63BC7 H

iv. The instruction queue of 8086 consists of **1**

(a) 6 data bytes (b) 8 data bytes

(c) 4 data bytes (d) 10 data bytes

v. IC 8255 provides I/O ports as follows **1**

(a) Four 8-bit ports

(b) Two 8-bit ports and one 6-bit port

(c) Two 8-bit port and a port divided into two groups of 4-bit each

(d) Two 6-bit ports and a port divided into two groups of 6-bit each

vi. IC 8253/8254 can be used to generate **1**
(a) Single pulse (b) Pulse train
(c) Square wave (d) All of these

vii. 8051 microcontroller has following **1**
(a) Two Timers and Two INTx pins
(b) Three Timers and Three INTx pins
(c) Two Timers and Three INTx pins
(d) Three Timers and Two INTx pins

viii. 8051 microcontroller does not have instruction for following operation **1**
(a) Multiply (b) Compare (c) Shift (d) Ex-OR

ix. Which processor has On-chip unified cache and Floating point unit **1**
(a) 8086 (b) 80186 (c) 80286 (d) 80486

x. ARM processor can fall into following class **1**
(a) RISC only (b) CISC only
(c) Both (a) and (b) (d) VLIW only

Q.2 Attempt any two :

i. Draw schematic diagram to show de-multiplexing of Address/ Data bus and Memory - I/O read/write signals with 8085. **5**

ii. Draw Timing diagram for instruction LXI H, 2500 H and explain T-state, machine cycle and Instruction cycle. **5**

iii. List different Features of memory mapped I/O and I/O mapped I/O schemes. **5**

Q.3 Attempt any two :

i. Explain different interrupts and related instructions in 8086. **5**

ii. Explain minimum operating modes of 8086. **5**

iii. Write 8086 assembly language program with proper comments to Arrange string of Ten words in Descending order. Assume arbitrary memory locations. **5**

Q.4 Attempt any two :

i. Draw block diagram of IC 8253/8254 and explain its operation. **5**

ii. What is the importance of DMA controller in a system? Explain Master/Slave role of DMA 8257. **5**

iii. Explain how USART 8251 is initialized for I/O data transfer in a processor system. **5**

Q.5 Attempt any two :

i. Explain any five bit-related instructions of 8051 with addressing mode, format and operation. **5**

ii. Explain different modes of operation of Timers in 8051 with associated function registers. **5**

iii. Explain with well commented program and neat interfacing diagram, how a desired message get displayed on LCD in 8051 system. **5**

Q.6 Attempt any two :

i. Explain the following **5**
(a) Von-neuman and Harvard architecture
(b) RISC and CISC processor

ii. Explain different features of processor 80286 with block architecture. **5**

iii. Draw Programming model of ARM microcontroller along with different Flags and their set/reset conditions. **5**

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Marking Scheme
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(c) All conditional flags

ii. In 8085 system, with I/O mapped I/O scheme Full address range for I/O devices and memory is **1**
(d) 256 Input,256 output and 64K memory

iii. In 8086, if content of IP register is 2057H, what will be the content of DS register to locate the physical address 43657H? **1**
(b) 4160 H

iv. The instruction queue of 8086 consists of **1**
(a) 6 data bytes

v. IC 8255 provides I/O ports as follows **1**
(c) Two 8-bit port and a port divided into two groups of 4-bit each

vi. IC 8253/8254 can be used to generate **1**
(d) All of these

vii. 8051 microcontroller has following **1**
(a) Two Timers and Two INTx pins

viii. 8051 microcontroller does not have instruction for following operation **1**
(c) Shift

ix. Which processor has On-chip unified cache and Floating point unit **1**
(d) 80486

x. ARM processor can fall into following class **1**
(c) Both (a) and (b)

Q.2 Attempt any two :

i. 8085 processor signals 1 mark **5**
Logic circuit for De-mutiplexing of Address/Data bus 2 marks
Logic circuit for De-mutiplexing of Memory - I/O read/write signals 2 marks

ii. Timing diagram with clock cycles for LXI H, 2500 H – opcode fetch, memory read, memory read 2.5 marks **5**
Definition of T-state, machine cycle and Instruction cycle. 2.5 marks

iii. Features of memory mapped I/O and I/O mapped I/O schemes. **5**
At least five features to compare both schemes
1 mark each (1 mark * 5)

Q.3 Attempt any two :

i. Different interrupts and related instructions in 8086. **5**
Type of interrupts 3 marks
Interrupt instruction 2 marks

ii. Explain minimum operating modes of 8086. **5**
Block diagram of minimum mode 2.5 marks
Explanation 2.5 marks

iii. 8086 assembly language program to arrange string of ten words in descending order 3 marks **5**
For logic applied (algorithm / flowchart) 1 mark
For proper comment 1 mark

Q.4 Attempt any two :

i. Neat and labelled block diagram of IC 8253/8254 2 marks **5**
Its operation 3 marks

ii. Importance of DMA controller in a system 2 marks **5**
Slave role of DMA 8257 1 mark
Master role of DMA 8257 2 marks

iii. Features of USART 8251 for I/O data transfer 1 marks **5**
Initialization control word format and explanation 2 marks
Mode format and explanation 2 marks

Q.5 Attempt any two :

i. Any five bit-related instructions of 8051 with addressing mode, format and operation. 1 mark each (1 mark * 5) **5**

	ii.	Modes 0,1,2 of operation of Timers in 8051		**5**
		1 mark each (1 mark * 3)	3 marks	
		Associated function registers TMOD , TCON	2 marks	
	iii.	Neat interfacing diagram with LCD	2 marks	**5**
		Program to display message on LCD	2 marks	
		Proper Comments	1 mark	
Q.6		Attempt any two :		
	i.	Explain the following		**5**
		(a) Von-neuman and Harvard architecture	2.5 marks	
		(b) RISC and CISC processor	2.5 marks	
	ii.	Different features of processor 80286	2.5 marks	**5**
		Block architecture.	2.5 marks	
	iii.	Programming model of ARM microcontroller	3 marks	**5**
		Different Flags and their set/reset conditions.	2 marks	

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