Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2018

CS3CO29/EC3CO07/EI3CO07/IT3CO09/OE00005

Digital Electronics

Programme: B.Tech. Branch/Specialisation: All

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Decimal 43 in hexadecimal and BCD number system is respectively **1**

(a) B2,0100 011 (b) 2B,0100 0011

(c) 2B,0011 0100 (d) B2,0100 0100

ii. A four-variable switching function has minterms m6 and m9. If the literals in these midterms are complemented, the corresponding minterm numbers are **1**

(a) m3 and m6 (b) m9 and m6

(c) m2 and m0 (d) m6 and m8

iii. The two-input of this gate is basically a modulo two adders **1**

(a) Ex-OR (b) OR gate (c) AND gate (d) NOR gate

iv. In a BCD adder circuit, a correction of **1**

(a) 1 is required (b) 3 is required

(c) 6 is required (d) 4 is required

v. The output Q_n of a J-K flip flop is zero. It changes to one (1) when a clock pulse is applied. The input J_n and K_n are respectively **1**

(a) 1 and x (b) 0 and x (c) x and 0 (d) x and 1

vi. A 4-bit synchronous counter uses flip flop with propagation delay time of 25ns each. The maximum possible time required for change of state will be **1**

(a) 25ns (b) 50ns (c) 75ns (d) 100ns

vii. Memory that is called a read write memory is **1**

(a) ROM (b) RAM (c) EPROM (d) EEPROM

P.T.O.

viii. PLA refers to **1**
(a) Programmable Loaded Array
(b) Programmable Logic Array
(c) Programmable Array Logic
(d) None of these

ix. TTL stands for **1**
(a) Transistor- Transmit Logic
(b) Transistor- Transistor Logic
(c) Transistor- Transfer Logic
(d) Transistor- Transistor Logical

x. Which is the fastest logic family **1**
(a) RTL (b) DTL (c) ECL (d) TTL

Q.2 i. Explain "Minterms & Don't care terms. **2**

ii. Convert the following: **3**
(a) $(1\ 0\ 1\ 1\ 1\ 1\ 0\ 1)_2 = (\ )_8$
(b) $(C\ 3\ A\ 6)_{16} = (\ )_2$
(c) $(3\ 7\ 0)_8 = (\ )_{16}$

iii. Express the following function in a sum of min-terms & product of max terms? Also implement using logic gates. **5**

$F(A, B, C) = (A + B)(B + C)$

OR iv. Find the minimal sum of products for the Boolean expression **5**

$F(A, B, C, D) = \Sigma m(1,2,3,7,8,9,10,11,14,15)$

using the Quine – McCluskey method.

Q.3 i. A combinational switching network has four inputs (A, B, C, D) and one output Z. The output is to be zero (0) if the input combination is a valid Excess 3 coded decimal digit. If any other combination of input is there output will be one (1). Design the network using basic gates. **3**

ii. For a full adder, first make the truth table & then using tabular method simplify the expression for sum and carry. Also draw the circuit for full adder. **7**

OR iii. Draw & explain the BCD adder circuit. **7**

Q.4 Attempt any two:

i. Explain the operation of a J-K flip-flop. What is meant by race around condition in J.K flip flop? **5**

ii. Design a mod-6 synchronous counter. **5**

iii. Realize a J-K flip-flop using S-R Flip-Flop. **5**

Q.5 i. Write short note on RAM. **4**

ii. Implement the function $F1=\sum(0,1,2,5,7)$ and $F2=\sum(1,2,4,6)$ using PROM. **6**

OR iii. Explain the PLA structure. **6**

Q.6 Attempt any two:

i. Draw & explain the circuit of a standard TTL. **5**

ii. Draw and explain how a CMOS logic circuit works. **5**

iii. Define the following: **5**
(a) Propagation delay time of a logic gate
(b) Figure of merit
(c) Fan out & Fan-in
(d) Noise Margin

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Marking Scheme

CS3CO29/EC3CO07/EI3CO07/IT3CO09/OE00005 Digital Electronics

Q.1	i.	Decimal 43 in hexadecimal and BCD number system is respectively (b) 2B,0100 0011		**1**
	ii.	A four-variable switching function has minterms m6 and m9. If the literals in these midterms are complemented, the corresponding minterm numbers are (b) m9 and m6		**1**
	iii.	The two-input of this gate is basically a modulo two adders (a) Ex-OR		**1**
	iv.	In a BCD adder circuit, a correction of (c) 6 is required		**1**
	v.	The output Q_n of a J-K flip flop is zero. It changes to one (1) when a clock pulse is applied. The input J_n and K_n are respectively (a) 1 and x		**1**
	vi.	A 4-bit synchronous counter uses flip flop with propagation delay time of 25ns each. The maximum possible time required for change of state will be (a) 25ns		**1**
	vii.	Memory that is called a read write memory is (b) RAM		**1**
	viii.	PLA refers to (b) Programmable Logic Array		**1**
	ix.	TTL stands for (b) Transistor- Transistor Logic		**1**
	x.	Which is the fastest logic family (c) ECL		**1**
Q.2	i.	Explanation of "Minterms Explanation of Don't care terms.	1 mark 1 mark	**2**
	ii.	Convert the following: 1 mark for each (a) $(1\ 0\ 1\ 1\ 1\ 1\ 0\ 1)_2 = (\ )_8$ (b) $(C\ 3\ A\ 6)_{16} = (\ )_2$ (c) $(3\ 7\ 0)_8 = (\ )_{16}$	(1 mark *3)	**3**
	iii.	Expression of sum of min-terms	2.5 marks	**5**
		Expression of Product of max terms	2.5 marks	
OR	iv.	For finding out expression $F(A,B,C,D) = \Sigma m(1,2,3,7,8,9,10,11,14,15)$ using the Quine – McCluskey method	5 marks	**5**
Q.3	i.	Designing Design using basic gates.	2 marks 1 mark	**3**
	ii.	Making the truth table Tabular method simplification of the expression for sum and carry Drawing of the circuit for full adder	2 marks 3 marks 2 marks	**7**
OR	iii.	Explanation the BCD adder circuit and designing. Truth table	5 marks 2 marks	**7**
Q.4		Attempt any two:		
	i.	Explanation of the operation a J-K flip-flop. Explanation of by race around condition in JK flip flop	2.5 marks 2.5marks	**5**
	ii.	Design a mod-6 synchronous counter.		**5**
	iii.	Realize a J-K flip-flop using S-R Flip-Flop.		**5**
Q.5	i.	Write short note on RAM.		**4**
	ii.	Implement the function $F1=\sum(0,1,2,5,7)$ and $F2=\sum(1,2,4,6)$ using PROM.	3 marks 3 marks	**6**
OR	iii.	Explain the PLA structure.		**6**
Q.6		Attempt any two:		
	i.	Explanation of the circuit of a standard TTL. Diagram	3 marks 2 marks	**5**
	ii.	Explanation of how a CMOS logic circuit works. Diagram	3 marks 2 marks	**5**
	iii.	Define the following: (a) Propagation delay time of a logic gate (b) Figure of merit (c) Fan out & Fan-in (d) Noise Margin	 1 mark 1 mark 2 marks 1 mark	**5**

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