Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2018

CS3CO22 Computer System Architecture

Programme: B.Tech. Branch/Specialisation: CSE

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. CPU has built-in ability to execute a particular set of machine instructions, called as _____ **1**

(a) Instruction Set (b) Registers
(c) Sequence Set (d) User instructions

ii. The ALU gives the output of the operations and the output is stored in the _____. **1**

(a) Memory Devices (b) Registers (c) Flags (d) Output Unit

iii. _____ converts the programs written in assembly language into machine instructions. **1**

(a) Compiler (b) Interpreter (c) Assembler (d) Converter

iv. What does the symbol '#' represent in the instruction MOV A, #50H? **1**

(a) Direct datatype (b) Indirect datatype
(c) Immediate datatype (d) Indexed datatype

v. The sign magnitude representation of -9 is _____. **1**

(a) 00001001 (b) 11111001 (c) 10001001 (d) 11001

vi. One extra bit is added on the left of a binary number, in case of Binary Multiplication using Booth's Algorithm. **1**

(a) True (b) False (c) May be (d) May not be

vii. Which of the following is true for a memory hierarchy? **1**

(a) It tries to bridge the processor memory speed gap.
(b) The speed of the memory level closest to the processor has the highest speed.
(c) It is based on the principle of locality of reference.
(d) All of these

P.T.O.

viii. In a virtual memory system, the address space specified by the address lines of the CPU must be _____ than the physical memory size, and _____ then the secondary storage size. **1**
(a) Smaller ,smaller (b) Smaller , larger
(c) Larger, smaller (d) Larger, larger

ix. Von Neumann architecture is **1**
(a) SISD (b) SIMD (c) MIMD (d) MISD

x. Which is used to speed-up the processing: **1**
(a) Pipeline (b) Vector processing
(c) Both (a) & (b) (d) None of these

Q.2 i. Draw Von-Neumann model of computer system and name its subsystems. **2**

ii. Define and explain following terms: **3**
(a) Registers
(b) Control Word
(c) ALU

iii. Explain different micro-operations with examples. **5**

OR iv. Explain various shift micro-operations with an example. **5**

Q.3 i. Define: **4**
(a) Bus structure
(b) Timing and control signals
(c) Interrupt
(d) Accumulator

ii. (a) What are the different fields of an instruction? Explain various instruction formats. **6**
(b) Explain instruction cycle with the help of flowchart.

OR iii. What do you mean by addressing modes of computer instructions? If an address field in an instruction contains decimal value 14, where is the corresponding operand located for following addressing modes? **6**
(a) Immediate addressing
(b) Direct addressing
(c) Indirect addressing
(d) Register addressing
(e) Register indirect addressing

Q.4 i. (a) Explain 2's complement method of subtraction of binary numbers. **4**
(b) How many bits are required to represent the following decimal numbers as unsigned binary integers?
(I) 12 (II) 147 (III) 384 (IV) 1497

ii. Draw flowchart to explain division algorithm for signed magnitude data. What is divide overflow condition? **6**

OR iii. Explain Booth's algorithm for multiplication of two fixed point numbers. Take two numbers of your choice for explaining the multiplication process. **6**

Q.5 i. Differentiate between synchronous and asynchronous data transfer. **2**

ii. What is DMA Controller? How it transfer data in a computer system? Explain. **3**

iii. Explain the need of cache memory. What is associative mapping technique in cache organization? **5**

OR iv. What is virtual memory? Explain concept of paging with the help of memory mapping table in a paged system. **5**

Q.6 i. Write in detail: **4**
(a) Advantages of parallel processing
(b) Inter processor communication

ii. Compare: **6**
(a) Array processor and vector processor
(b) RISC processor and CISC processor

OR iii. Explain the following: **6**
(a) Flynn's classification
(b) Pipelining

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Marking Scheme
CS3CO22 Computer System Architecture

Q.1 i. CPU has built-in ability to execute a particular set of machine instructions, called as _____ **1**
(a) Instruction Set

ii. The ALU gives the output of the operations and the output is stored in the _____. **1**
(b) Registers

iii. _____ converts the programs written in assembly language into machine instructions. **1**
(c) Assembler

iv. What does the symbol '#' represent in the instruction MOV A, #50H? **1**
(c) Immediate datatype

v. The sign magnitude representation of -9 is _____. **1**
(c) 10001001

vi. One extra bit is added on the left of a binary number, in case of Binary Multiplication using Booth's Algorithm. **1**
(a) True

vii. Which of the following is true for a memory hierarchy? **1**
(d) All of these

viii. In a virtual memory system, the address space specified by the address lines of the CPU must be _____ than the physical memory size, and _____ then the secondary storage size. **1**
(c) Larger, smaller

ix. Von Neumann architecture is **1**
(a) SISD

x. Which is used to speed-up the processing: **1**
(c) Both (a) & (b)

Q.2 i. Diagram of VonNeumann model 1 mark **2**
Name of its subsystems 1 mark

ii. Define and explain following terms: **3**
(a) Registers 1 mark
(b) Control Word 1 mark
(c) ALU 1 mark

iii. Explain different microoperations with examples. **5**
Definition and types 1 mark
Examples of each categories with description 4 marks

OR iv. Name (Any Four) 1 mark **5**
Example 1 mark for each (1 mark * 4) 4 marks

Q.3 i. Define: **4**
(a) Bus structure 1 mark
(b) Timing and control signals 1 mark
(c) Interrupt 1 mark
(d) Accumulator 1 mark

ii. (a) What are the different fields of an instruction? Explain various instruction formats. 3 marks **6**
(b) Explain instruction cycle with the help of flowchart. 3 marks

OR iii. What do you mean by addressing modes of computer instructions? If an address field in an instruction contains decimal value 14, where is the corresponding operand located for following addressing modes? **6**
(a) immediate addressing?
(b) direct addressing?
(c) indirect addressing?
(d) register addressing?
(e) register indirect addressing?
Definition of addressing modes 1 mark
Each option (1 mark * 5) 5 marks

Q.4 i. Explain 2's complement method of subtraction of binary numbers. **4**
2's complement representation 1 mark
Subtraction example 1 mark
How many bits are required to represent the following decimal numbers as unsigned binary integers? 0.5 marks for each 2 marks
(a) 12 - 4 bits
(b) 147 - 8 bits
(c) 384 - 9 bits
(d) 1497 – 11 bits

ii. Draw flowchart to explain division algorithm for signed magnitude data. What is divide overflow condition? **6**
Flowchart 3 marks
Explanation 2 marks
Divide overflow 1 mark

OR iii. Booth's algorithm and Flowchart 4 marks **6**
Example 2 marks

Q.5 i. Differentiate between synchronous and asynchronous data transfer. **2**
Differences (at least 3) 2 marks

ii. What is DMA Controller? How it transfer data in a computer system? Explain. **3**

Definition and explanation 1 mark
Working 2 marks

iii. Explain the need of cache memory. What is associative mapping technique in cache organization? **5**

Need of cache memory 2 marks
Associative mapping 3 marks

OR iv. What is virtual memory? Explain concept of paging with the help of memory mapping table in a paged system. **5**

Definition 1 mark
Paging concept 2 marks
Diagram 2 marks

Q.6 i. Write in detail: **4**

(a) Advantages of parallel processing 2 marks
(b) Inter processor communication 2 marks

ii. Compare: **6**

(a) Array processor and vector processor 3 marks
(b) RISC processor and CISC processor 3 marks

OR iii. Explain the following: **6**

(a) Flynn's classification 3 marks
(b) Pipelining 3 marks

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