Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2017

CS3CO02 Computer Architecture and Organization

Programme: B.Tech. Branch/Specialisation: CS

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. The component of computer responsible for controlling and coordinating operations. **1**

(a) ALU (b) Memory (c) I/O (d) CU

ii. Where the result of an arithmetic and logical operation are stored? **1**

(a) In Accumulator (b) In Cache Memory

(c) In ROM (d) In Instruction Register

iii. After counting 0, 1, 10, 11, the next binary number is **1**

(a) 12 (b) 100 (c) 101 (d) 110

iv. Convert binary 111111110010 to hexadecimal. **1**

(a) $(EE2)_{16}$ (b) $(FF2)_{16}$ (c) $(2FE)_{16}$ (d) $(FD2)_{16}$

v. After the device completes its operation _____ assumes the control of the BUS. **1**

(a) Another device (b) Processor

(c) Controller (d) None of these

vi. The pipelining process is also called as _____. **1**

(a) Superscalar operation (b) Assembly line operation

(c) Von Neumann cycle (d) None of these

vii. The BOOT sector files of the system are stored in _____. **1**

(a) Hard disk

(b) RAM

(c) ROM

(d) Fast solid state chips in the other board

viii. The _____ process divides the disk into sectors and tracks. **1**

(a) Creation (b) Initiation (c) Formatting (d) Modification

ix. Any condition that causes a processor to stall is called as _____. **1**
(a) Hazard (b) Page fault
(c) System error (d) None of these

x. In the client server model of the cluster _____ approach is used. **1**
(a) Load configuration (b) FIFO
(c) Bankers algorithm (d) Round robin

Q.2 i. What, in general terms, is the distinction between computer organization and computer architecture? **2**

ii. List and briefly define the main structural components of a computer. **3**

iii. Write and explain various addressing modes of basic computer. **5**

OR iv. Explain in brief computer generation. **5**

Q.3 Attempt any two:

i. Write single precision floating point representation of positive binary number $(111.10101)_2 * 2^5$. **5**

ii. Explain sign magnitude, 1's complement and 2's compliment with a suitable example. **5**

iii. Write detailed procedure for Decimal to Hexadecimal conversion and Hexadecimal to Octal conversion. **5**

Q.4 i. Consider a pipeline with 5 stages. Assume the 1^{st} stage takes 5 units of time, 2^{nd} takes 2 units of time, 3^{rd} takes 3 unit of time, 4^{th} takes 1 unit of time and 5^{th} takes 4 unit of time. Calculate speed up factor of pipeline over non pipeline. **4**

ii. Explain Vector, Array and Multithreaded processor. **6**

OR iii. Explain hardwired control unit and differentiate horizontal & vertical micro programmed control unit. **6**

Q.5 Attempt any two:

i. A moving arm disk-storage device has the following specifications: **5**
Number of tracks per recording surface -200,
Disk – rotation speed – 2400 rpm,
Track storage capacity – 62,500 bits.
What is the data transfer rate (in kilo bytes/sec) for this device?

ii. Explain in brief memory hierarchy with suitable diagram. **5**

iii. List and explain at least five auxiliary memory peripheral devices. **5**

Q.6 Attempt any two:

i. Describe Flynn's classification for multiprocessor organization. **5**

ii. What do you understand by inter-processor communication? Describe with suitable diagram. **5**

iii. What are Multi-core processors? Describe the architecture of any one of multi-core processor. **5**

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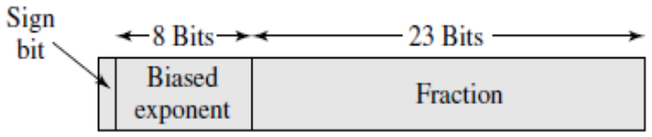
CS3CO02 Computer Architecture and Organization

Marking Scheme

Q.1 i. (d) CU **1**
ii. (a) In Accumulator **1**
iii. (b) 100 **1**
iv. (b) $(FF2)_{16}$ **1**
v. (b) Processor **1**
vi. (b) Assembly line operation **1**
vii. (c) ROM **1**
viii. (c) Formatting **1**
ix. (a) Hazard **1**
x. (d) Round robin **1**

Q.2 i. Computer organization [1 Marks] and computer architecture[1 Marks] **2**
ii. List [1 Marks] structural components [2 Marks] **3**
iii. 5 addressing mode of 1 mark each **5**
OR iv. 5 generations 1 mark each **5**

Q.3 i. Single Precision Format **5**



$(111.10101)_2 * 2^5 = 1.1110101 * 2^7$(normalized)
Sign bit = 0
Biased exponent (excess 127 method) = 127+7 = 134 =$(10000110)_2$
Mantissa (only fraction part 23 bit) = 11101010000000000000000
Answer = 0 10000110 11101010000000000000000

ii. Sign magnitude[1 Marks], 1's complement[2 Marks] and 2'scompliment[2 Marks] **5**
OR iii. Decimal to Hexadecimal conversion [2.5 Marks] and Hexadecimal to Octal conversion[2.5 Marks] **5**

Q.4 i. **4**

$$\text{Speed up} = \frac{t_n}{t_p} = \frac{(5+2+3+1+4)}{5} = \frac{15}{5} = 3$$

($\because$ t_p: Maximum time unit of all stages + overhead $\rightarrow$ overhead is zero here)

ii. Vector [2 Marks], Array [2 Marks] and Multithreaded processor [2 Marks]. **6**
OR iii. Hardwired control unit [2 Marks] and differentiate horizontal & vertical micro programmed control unit [4 Marks]. **6**

Q.5 i. **5**

$$1 \text{ rotation} - \frac{1}{40}\text{sec}\ ;\ \frac{1}{40}\text{sec} - 62500\text{bits}$$

$$1\text{sec} - 62500 \times 40\text{bits}$$

$$= \frac{62500 \times 40}{1000 \times 8}\text{k bytes}$$

$$= \frac{625}{2} = 312.5\text{k bytes}$$

ii. Memory hierarchy [3 Marks] diagram [2 Marks]. **5**
OR iii. List [1 Marks] and explain at least 5 auxiliary memory peripheral devices [4 Marks]. **5**

Q.6 Attempt any two:
i. Flynn's classification [5 Marks] **5**
ii. Inter-processor communication [3 Marks] diagram [2 Marks]. **5**
iii. Multi-core processors[3 Marks] architecture of any one of multi-core processor[2 Marks] **5**

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