Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Engineering

End Sem (Odd) Examination Dec-2017

CS2CO04 Computer Organization & Architecture

Programme: Diploma Branch/Specialisation: CS

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. CPU does not perform the operation..... **1**

(a) Data Transfer (b) Logic Operation

(c) Arithmetic Operation (d) All of these

ii. A group of bits that tell the computer to perform a specific operation is known as **1**

(a) Register (b) Micro-Operation

(c) Accumulator (d) Instruction Code

iii. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be **1**

(a) $(12)_{10}$ (b) $(-12)_{10}$ (c) $(812)_{10}$ (d) $(-812)_{10}$

iv. A floating point number that has a O in the MSB of mantissa is said to have **1**

(a) Overflow (b) Underflow

(c) Important number (d) Undefined

v. Memory access in RISC architecture is limited to instructions **1**

(a) CALL and RET (b) PUSH and POP

(c) STA and LDA (d) MOV and JMP

vi. In Reverse Polish notation, expression A*B+C*D is written as **1**

(a) AB*CD*+ (b) A*BCD*+

(c) AB*CD+* (d) A*B*CD+

vii. An interface that provides I/O transfer of data directly to and from the memory unit and peripheral is termed as **1**

(a) DDA (b) Serial interface

(c) BR (d) DMA

P.T.O

	viii.	Memory unit accessed by content is called (a) Read only memory (b) Associative Memory (c) Virtual Memory (d) Programmable Memory		**1**
	ix.	An instruction pipeline can be implemented by means of (a) LIFO buffer (b) Stack (c) FIFO buffer (d) None of these		**1**
	x.	Data hazards occur when..... (a) Greater performance loss. (b) Pipeline changes the order of read/write access to operands. (c) Some functional unit is not fully pipelined. (d) Machine size is limited.		**1**
Q.2	i.	Draw a block diagram of digital computer.		**2**
	ii.	What is Register Transfer Language?		**3**
	iii.	Explain Von-Neumann model for computation.		**5**
OR	iv	What is difference between instruction and Micro- Operation? List types of Micro- Operation and explain them.		**5**
Q.3	i.	Write the procedure to find 1's and 2's complement of a binary number.		**2**
	ii.	Explain BCD adder with the block diagram.		**3**
	iii.	Discuss Multiplication Algorithm with the flow chart.		**5**
OR	iv.	Explain floating point representation with example. (a) Instruction Format (b) Stack Organization		**5**
Q.4	i.	Explain control word with example.		**2**
	ii.	What are the differences between RISC and CISC architecture?		**3**
	iii.	Define following terms in brief: (a) Two address instructions (b) Three address instructions		**5**
OR	iv.	Write and explain various addressing modes of basics computer.		**5**
Q.5	i.	Define the term Priority Interrupt.		**2**
	ii.	Draw and explain typical block diagram of DMA?		**3**
	iii.	Explain associative memory with its hardware organization. Explain how the data is read and write in the associative memory.		**5**

OR	iv.	What are the various mapping methods used with cache memory organization? Explain any one in brief.		**5**
Q.6	i.	Explain the basic structure of pipeline processor.		**2**
	ii.	What is parallel processing? Explain the significance of parallel processing		**3**
	iii.	Give a summary of arithmetic and logical operation that are defined for the vector architecture.		**5**
OR	iv.	Write short notes: (a) Memory Interleaving (b) Matrix Multiplication		**5**

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Marking Scheme

Q.1	i.	(a) Data Transfer	**1**
	ii.	(d) Instruction Code	**1**
	iii.	(c) (812) 10	**1**
	iv.	(b) Underflow	**1**
	v.	(c) STA and LDA	**1**
	vi.	(a) AB*CD*+	**1**
	vii.	(d) DMA	**1**
	viii.	(b) Associative Memory	**1**
	ix.	(c) FIFO buffer	**1**
	x.	(b) Pipeline changes the order of read/write access to operands	**1**
Q.2	i.	Draw a block diagram of digital computer. (2 mark for diagram)	**2**
	ii.	What is Register Transfer Language? (1 marks for definition and 2 marks for description)	**(1+2)=3**
	iii.	Explain Von-Neumann model for computation. (3 mark for answer 2 mark for diagram)	**(3+2)=5**
OR	iv	What is difference between instruction and Micro- Operation? Micro- Operation? List types of Micro- Operation and explain them (2 mark for difference 3 mark for types)	**(2+3)=5**
Q.3	i.	Write the procedure to find 1's and 2's complement of a binary number. (1 mark for 1's and 1 mark for 2's)	**(1+1)=2**
	ii.	Explain BCD adder with the block diagram. (1 mark for definition and 2 marks for diagram)	**(1+2)=3**
	iii.	Discuss Multiplication Algorithm with the flow chart. (3 mark for answer 2 mark for diagram)	**(3+2)=5**
OR	iv.	Explain floating point representation with example. (3 mark for answer 2 mark for example)	**(3+2)=5**
Q.4	i.	Explain control word with example. (1 marks for definition & 1 mark for description)	**(1+1)=2**
	ii.	What are the differences between RISC and CISC architecture? (3 mark for difference)	**3**
	iii.	Define following terms in brief: (a) Instruction Format (2.5 mark) (b) Stack Organization (2.5 mark)	**(2.5+2.5)=5**
OR	iv.	Write and explain various addressing modes of basics computer. (2 mark for description and 3 mark for types)	**(2+3)=5**
Q.5	i.	Define the term Priority Interrupt. (2 mark for definition)	**2**
	ii.	Draw and explain typical block diagram of DMA? (1 marks for definition and 2 marks for diagram, description)	**(1+2)=3**
	iii.	Explain associative memory with its hardware organization. Explain how the data is read and write in the associative memory. (3 mark for description and 2 mark for read/write)	**(3+2)=5**
OR	iv.	What are the various mapping methods used with cache memory organization? Explain any one in brief. (3 mark for definition, types & 2 mark for one description)	**(3+2)=5**
Q.6	i.	Explain the basic structure of pipeline processor. (1 marks for structure & 1 mark for description)	**(1+1)=2**
	ii.	What is parallel processing? Explain the significance of parallel processing (1 mark for definition & 2 mark for types)	**(1+2)=3**
	iii.	Give a summary of arithmetic and logical operation that are defined for the vector architecture. (2 mark for definition & 3 mark for description)	**(2+3)=5**
OR	iv.	Write short notes: (a) Memory Interleaving (2.5 mark) (b) Matrix Multiplication (2.5 mark)	**(2.5+2.5)=5**

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