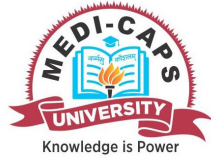


Enrollment No.....



Faculty of Engineering

End Sem (Odd) Examination Dec-2018

CA5CO03 Computer Organization & Architecture

Programme: MCA

Branch/Specialisation: Computer
Application**Duration: 3 Hrs.****Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

- Q.1 i. Convert the following binary number to decimal. 01011_2 **1**
(a) 15 (b) 18 (c) 14 (d) 11
- ii. Which of the following is the most widely used alphanumeric code for computer input and output? **1**
(a) GRAY (b) ASCII (c) PARITY (d) EBCDIC
- iii. Which language is termed as the symbolic depiction used for indicating the series: **1**
(a) Random transfer language
(b) Register transfer language
(c) Arithmetic transfer language
(d) All of these
- iv. Which are the operation that a computer performs on data that put in register: **1**
(a) Register transfer (b) Arithmetic
(c) Logical (d) All of these
- v. The DMA controller has _____ registers **1**
(a) 4 (b) 2 (c) 3 (d) 1
- vi. The technique whereby the DMA controller steals the access cycles of the processor to operate is called **1**
(a) Fast conning (b) Memory Con
(c) Cycle stealing (d) Memory stealing
- vii. Which of the following is a 16-bit register? **1**
(a) AL (b) AX (c) AH (d) All of these

- viii. The number of address and data lines of 8086 _____ **1**
(a) 8 and 8 (b) 16 and 16 (c) 20 and 16 (d) 16 and 20
- ix. SDRAM stands for: **1**
(a) System dynamic random access memory
(b) Synchronous dynamic random access memory
(c) Both (a) and (b)
(d) None of these
- x. The memory bus is also referred as _____: **1**
(a) Data bus (b) Address bus
(c) Memory bus (d) All of these

- Q.2 i. Convert $(108)_{10}$ into binary, octal, and Hexadecimal. **3**
ii. Draw and explain 16×1 Multiplexer. **7**
- OR iii. Define and explain Boolean Variable, Boolean algebra, Boolean expression and logic diagram with example. **7**
- Q.3 i. What do you mean by micro operation? Explain giving example. **3**
ii. Draw and explain 4-bits arithmetic circuit **7**
- OR iii. What is register transfer? Explain unconditional and conditional transfer giving example of each. **7**
- Q.4 i. What do you mean by zero, one and two address instructions? Explain with suitable example. **3**
ii. What do you mean by instruction set of computer? Explain when the instruction set is said to be complete. **7**
- OR iii. Explain hardwired implementation of control unit. **7**
- Q.5 i. What are the features of 8086? **4**
ii. Draw the block diagram of 8086. Explain in brief. **6**
- OR iii. Explain different addressing modes in 8086. **6**
- Q.6 Attempt any two: **5**
i. Explain different types of ROM. **5**
ii. Build 256×8 using 128×8 chips. **5**
iii. Explain contemporary memory hierarchy structure. **5**

Marking Scheme

CA5CO03 Computer Organization & Architecture

Q.1	i. Convert the following binary number to decimal. 01011_2 (d) 11	1	
	ii. Which of the following is the most widely used alphanumeric code for computer input and output? (b) ASCII	1	
	iii. Which language is termed as the symbolic depiction used for indicating the series: (b) Register transfer language	1	
	iv. Which are the operation that a computer performs on data that put in register: (d) All of these	1	
	v. The DMA controller has _____ registers (c) 3	1	
	vi. The technique whereby the DMA controller steals the access cycles of the processor to operate is called (c) Cycle stealing	1	
	vii. Which of the following is a 16-bit register? (b) AX	1	
	viii. The number of address and data lines of 8086 _____ (c) 20 and 16	1	
	ix. SDRAM stands for: (b) Synchronous dynamic random access memory	1	
	x. The memory bus is also referred as _____: (a) Data bus	1	
Q.2	i. Convert $(108)_{10}$ into binary Octal Hexadecimal.	1 mark 1 mark 1 mark	3
	ii. Draw 16×1 Multiplexer Explanation	3 marks 4 marks	7
OR	iii. Definition Boolean algebra Boolean expression Logic diagram	1 mark 2 marks 2 marks 2 marks	7
Q.3	i. Micro operation Example.	2 marks 1 mark	3
	ii. Draw 4-bits arithmetic circuit Explanation	3 marks 4 marks	7
	OR iii. Register transfer Unconditional and conditional transfer	3.5 marks 3.5 marks	7
Q.4	i. Zero, one and two address instructions with example 1 mark for each	(1 mark * 3)	3
	ii. Instruction set of computer When the instruction set is said to be complete	3.5 marks 3.5 marks	7
	OR iii. Hardwired implementation of control unit. Diagram Explanation	3.5 marks 3.5 marks	7
Q.5	i. Features of 8086? ii. Block diagram of 8086 Explanation	3 marks 3 marks	4 6
	OR iii. Different addressing modes in 8086. Explanation	2 marks 4 marks	6
Q.6	Attempt any two: i. Different types of ROM. Definition Explanation of types	2 marks 3 marks	5
	ii. Build 256×8 using 128×8 chips. Diagram Explanation	2 marks 3 marks	5
	iii. Contemporary memory hierarchy structure. Diagram Explanation	2 marks 3 marks	5
