Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Science

End Sem (Odd) Examination Dec-2018

CA3CO02 Digital Electronics

Programme: BCA Branch/Specialisation: Computer Application

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Simplified expression of full subtractor borrow is **1**

(a) B=xy+xz+yz (b) B=xy'+xz'+yz

(c) B=x'y+xy+xz (d) B=x'y+x'z+yz

ii. Binary parallel adder can be used as both adder and subtraction circuit using which of the following gate. **1**

(a) AND gate (b) OR gate (c) XOR gate (d) NOT gate

iii. The output of an AND gate with three inputs, A, B, and C, is HIGH when **1**

(a) A = 1, B = 1, C = 0 (b) A = 0, B = 0, C = 0

(c) A = 1, B = 1, C = 1 (d) A = 1, B = 0, C = 1

iv. If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output? **1**

(a) 1 (b) 2 (c) 7 (d) 8

v. Which statement BEST describes the operation of a negative-edge-triggered D flip-flop? **1**

(a) The logic level at the D input is transferred to Q on NGT of CLK.

(b) The Q output is ALWAYS identical to the CLK input if the D input is HIGH.

(c) The Q output is ALWAYS identical to the D input when CLK = PGT.

(d) The Q output is ALWAYS identical to the D input.

P.T.O.

vi. How many flip-flops are in the 7475 IC? **1**
(a) 1 (b) 2 (c) 4 (d) 8

vii. The terminal count of a modulus-11 binary counter is **1**
(a) 1010 (b) 1000
(c) 1001 register (d) 1100

viii. Synchronous construction reduces the delay time of a counter to the delay of: **1**
(a) All flip-flops and gates
(b) All flip-flops and gates after a 3 count
(c) A single gate
(d) A single flip-flop and a gate

ix. Component most likely used for computer static RAM technology is **1**
(a) Primary memory (b) Secondary storage
(c) Cache memory (d) CPU registers

x. Computer memory which allows simultaneous read and write operations is **1**
(a) ROM (b) RAM (c) EPROM (d) EEPROM

Q.2 i. How can we design NOT and OR gate with the help of NAND gate? Explain with the help of diagram. **4**
ii. Write and prove De-Morgan theorem. **6**
OR iii. Simplify the following Boolean function using K-map. **6**
$F(A,B,C) = \sum m(0,1,4,5) = A'B'C' + A'B'C + AB'C' + AB'C$

Q.3 i. Convert the binary code 01001 into its equivalent grey code. **2**
ii. What is Excess-3 Code? Give examples. Show how it is useful for BCD addition. **8**
OR iii. Convert following: **8**
(a) $(231)_8 \longrightarrow (\ )_{16}$ (b) $(11.85)_{10} \longrightarrow (\ )_8$
(c) $(7DE)_{16} \longrightarrow (\ )_{10}$ (d) $(17.75)_8 \longrightarrow (\ )_2$

Q.4 i. What is meant by D-flip flop? Explain. **3**
ii. Design a SR flip flop using NAND gate. **7**

OR iii. Write a short note on: - **7**
(a) Adder/subtractor (b) Encoder /decoder

Q.5 i. Explain shift register with its types. **4**
ii. Design a 3 bit asynchronous up counter. **6**
OR iii. Explain D/A Converters and A/D Converters. **6**

Q.6 Attempt any two:
i. Explain Secondary Memory with Its Types. **5**
ii. What is ROM? Difference between EPROM & EEPROM. **5**
iii. Write various types of RAM and explain them in brief. **5**

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Marking Scheme
CA3CO02 Digital Electronics

Q.1	i.	Simplified expression of full subtractor borrow is (d) B=x'y+x'z+yz		**1**
	ii.	Binary parallel adder can be used as both adder and subtraction circuit using which of the following gate. (c) XOR gate		**1**
	iii.	The output of an AND gate with three inputs, A, B, and C, is HIGH when (c) A = 1, B = 1, C = 1		**1**
	iv.	If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output? (a) 1		**1**
	v.	Which statement BEST describes the operation of a negative-edge-triggered D flip-flop? (a) The logic level at the D input is transferred to Q on NGT of CLK.		**1**
	vi.	How many flip-flops are in the 7475 IC? (c) 4		**1**
	vii.	The terminal count of a modulus-11 binary counter is (a) 1010		**1**
	viii.	Synchronous construction reduces the delay time of a counter to the delay of: (d) A single flip-flop and a gate		**1**
	ix.	Component most likely used for computer static RAM technology is (c) Cache memory		**1**
	x.	Computer memory which allows simultaneous read and write operations is (b) RAM		**1**
Q.2	i.	Design NOT gate with the help of NAND gate	2 marks	**4**
		Design OR gate with the help of NAND gate	2 marks	
	ii.	De-Morgan theorem diagram	2 marks	**6**
		Description	4 marks	
OR	iii.	Boolean function using K-map.	2 marks	**6**
		Simplification of expression	4 marks	
Q.3	i.	Convert the binary code 01001 into its equivalent grey code.		**2**
	ii.	Excess-3 Code	2.5 marks	**8**
		Example of Excess-3 Code	2.5 marks	
		Excess-3 Code useful for BCD addition	3 marks	
OR	iii.	Convert following:Each conversion 2 marks	(2 marks *4)	**8**
		(a) $(231)_8 \rightarrow (\ )_{16}$ (b) $(11.85)_{10} \rightarrow (\ )_8$		
		(c) $(7DE)_{16} \rightarrow (\ )_{10}$ (d) $(17.75)_8 \rightarrow (\ )_2$		
Q.4	i.	Description of D-flip flop	2 marks	**3**
		Diagram	1 mark	
	ii.	Description of SR flip flop	2 marks	**7**
		Truth table of NAND gate	2 marks	
		Diagram of SR flip flop	3 marks	
OR	iii.	Write a short note on: -		**7**
		(a) Adder/subtractor	3.5 marks	
		(b) Encoder /decoder	3.5 marks	
Q.5	i.	Shift register	2 marks	**4**
		Its types	2 marks	
	ii.	3 bit asynchronous up counter description	3 marks	**6**
		Diagram	3 marks	
OR	iii.	D/A Converters description	3 marks	**6**
		A/D Converters description	3 marks	
Q.6		Attempt any two:		
	i.	Secondary Memory description	2 marks	**5**
		Its Types	3 marks	
	ii.	ROM description	2 marks	**5**
		Difference b/w EPROM & EEPROM		
		Any three points 1 mark each	3 marks	
	iii.	Ram description	2 marks	**5**
		Types of RAM	3 marks	

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