Total No. of Questions: 6 *Total No. of Printed Pages:3*

Enrollment No.....

Faculty of Science

End Sem (Odd) Examination Dec-2017

BC3CO10 Computer Organization

Programme: B.Sc.(CS) Branch/Specialisation: Computer Science

Duration: 3 Hrs. **Maximum Marks: 60**

Note: All questions are compulsory. Internal choices, if any, are indicated. Answers of Q.1 (MCQs) should be written in full instead of only a, b, c or d.

Q.1 i. Where does a computer add and compare data? **1**

(a) Hard disk (b) Floppy disk

(c) CPU (d) Memory chip

ii. Different components on the motherboard of a PC unit are linked together by sets of parallel electrical conducting lines. What are these lines called? **1**

(a) Conductors (b) Buses

(c) Connectors (d) Consecutives

iii. _____ register keeps tracks of the instructions stored in program stored in memory. **1**

(a) AR (Address Register) (b) XR (Index Register)

(c) PC (Program Counter) (d) AC (Accumulator)

iv. In a vectored interrupt **1**

(a) The branch address is assigned to a fixed location in memory.

(b) The interrupting source supplies the branch information to the processor through an interrupt vector.

(c) The branch address is obtained from a register in the processor

(d) None of the above

v. The DMA transfers are performed by a control circuit called as **1**

(a) Device interface (b) DMA controller

(c) Data controller (d) Overlooker

vi. _____is a dedicated processor that combines interface unit and DMA as one unit. **1**

(a) Input-Output Processor (b) Only input processor

(c) Only output processor (d) None of these

P.T.O.

vii. The idea of cache memory is based **1**
(a) On the property of locality of reference
(b) On the heuristic 90-10 rule
(c) On the fact that references generally tend to cluster
(d) All of the above

viii. Memory unit accessed by content is called **1**
(a) Read only memory (b) Programmable Memory
(c) Virtual Memory (d) Associative Memory

ix. The Intel 8086 microprocessor is a _____ processor **1**
(a) 4 bit (b) 8 bit (c) 16 bit (d) 32 bit

x. Data hazards occur when..... **1**
(a) Greater performance loss
(b) Pipeline changes the order of read/write access to operands
(c) Some functional unit is not fully pipelined
(d) Machine size is limited

Q.2 i. Explain the functional units of a digital computer **4**
ii. With appropriate diagrams explain the bus structure of a computer. **6**
OR iii. What are the factors that determine the performance of a computer? **6**

Q.3 i. Compare register reference and memory reference instruction. **4**
ii. List the various computer registers and specify purpose of each register. **6**
OR iii. What is an interrupt? Explain the steps to be carried out while serving an interrupt. **6**

Q.4 i. What is the need for an interface between an I/O device and the CPU? **2**
ii. Compare synchronous and asynchronous transfer modes. **3**
iii. Explain various ways of implementing priority interrupt. **5**
OR iv. Explain CPU-IOP communication. **5**

Q.5 i. Why the size of cache and main memory are related? **2**
ii. What is page fault? How it is handled? **3**
iii. What is virtual memory? Explain with a diagram how virtual address can be mapped into physical address using paging. **5**
OR iv. Explain the basic operation of the cache memory. **5**

Q.6 Write short note on any two:
i. Register Organization of microprocessor 8086 **5**
ii. Pipeline Hazards **5**
iii. Pipelining in Pentium **5**

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Marking Scheme

Q.1	i.	(c) CPU	**1**
	ii.	(b) Buses	**1**
	iii.	(c) PC (Program Counter)	**1**
	iv.	(b) The interrupting source supplies the branch information to the processor through an interrupt vector.	**1**
	v.	(b) DMA controller	**1**
	vi.	(a) Input-Output Processor	**1**
	vii.	(a) On the property of locality of reference	**1**
	viii.	(d) Associative Memory	**1**
	ix.	(c) 16 bit	**1**
	x.	(b) Pipeline changes the order of read/write access to operands	**1**
Q.2	i.	Functional units of a digital computer **(1 mark + 3 marks)**	**4**
	ii.	Diagrams explain the bus structure of a computer system. **(2 mark + 4 marks)**	**6**
OR	iii.	Factors that determine the performance of a computer **(2 mark + 4 marks)**	**6**
Q.3	i.	Register reference – **2 marks** Memory reference – **2 marks**	**4**
	ii.	For Listing registers - **2 marks** For purpose register - **4 marks**	**6**
OR	iii.	Interrupt - **2 marks** Steps of interrupt. – **4 marks**	**6**
Q.4	i.	Need for an interface between an I/O device and the CPU	**2**
	ii.	Synchronous transfer modes – **1.5 marks** Asynchronous transfer modes. – **1.5 marks**	**3**
	iii.	Ways of implementing priority interrupt.	**5**
OR	iv.	CPU-IOP communication.	**5**
Q.5	i.	Reason of relation between size of cache and main memory	**2**
	ii.	Page fault – **1.5 marks** Handling – **1.5 marks**	**3**
	iii.	Virtual memory – **1 marks** Explanation with a diagram – **4 marks**	**5**
OR	iv.	Basic operation of the cache memory.	**5**
Q.6		Attempt any two:	
	i.	Register Organization of microprocessor 8086	**5**
	ii.	Pipeline Hazards	**5**
	iii.	Pipelining in Pentium	**5**

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